## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application Serial No	10/769.573
Filing Date	January 30, 2004
Inventorship	
Assignee	
Group Art Unit	
Examiner	
Attorney's Docket No	
Customer No.	
Title: Gated Semiconductor Assemblies a	nd Methods of Forming Gate
Semiconductor Assemblies	•

Semiconductor Assemblies

## SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

References - See Attached Form PTO-1449

In compliance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, your attention is directed to the United States patents and other references listed on the attached Form PTO-1449. No admission is made regarding whether all the submitted references are prior art.

This Supplemental Information Disclosure Statement is being filed together with a Request for Continued Examination application. Therefore, no fee is believed to be required. However, in the event that a fee is required for filing this Supplemental Information Disclosure Statement, please charge the fee specified under 37 C.F.R. § 1.17(p) to Deposit Account No. 23-0925.

Respectfully submitted,

Dated: 30 Mev 2005

By:

Reg. No. 44,854

Form PTO-1449			U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE			ATTY. DOCKET NO. MI22-2478			SERIAL NO. 10/769,573		
	Z	LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)			APPLICANT: Mark A. Helm						
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U.S. PATENT DOCUMENTS											
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	AJ	JP409055351A	02/1997	Japan (and Abstract)					100	X	
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